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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,917	10/04/1999	NAOMI YAMAZAKI	FUJO-16.572	8953

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EXAMINER	
TRAN, THIEN D	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/411,917	YAMAZAKI, NAOMI	
	Examiner	Art Unit	
	Thien D Tran	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *15*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8 are rejected under 35 U.S.C. 102(b) as being unpatentable over Yamazaki (U.S Patent No. 4,841,522).

Regarding claim 1, Yamazaki discloses a cross-connection switch comprising:

control memory (first memory mean) for storing data indicating switching information of a time slot at an address to which time slot information is assigned (col.2 lines 15-25);

channel memory (second memory means) for storing data of each time slot of an input frame in time slot units, inputting data stored in said first memory means, and outputting the data stored at the address specified by the data as time slot data of an output frame (col.2 lines 15-25); and

counter means for counting a number of input time slots of an input frame in synchronization with the input frame, and outputting the count value as a read address and a write address respectively to said first memory means and said second memory means (col.2 lines 15-25, figure 1).

Regarding claim 2, Yamazaki discloses a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n-bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means (col.2 lines 45-55).

Regarding claim 3, Yamazaki discloses a plurality of lines are accommodated by said cross-connection switch, any line of the plurality of lines is selected for a switching process by entering switching information about time order of data of a time slot and switching information data between lines at each address of said first memory means (col.3 line 40 to col.4 line 25).

Regarding claim 4, Yamazaki discloses that information of a current input time slot is written to said second memory means, data to be used in processing one time slot before the current input time slot is read from said first memory means, a read address is output from said first memory means to said second memory means, and time slot data used in processing the one time slot before the current input time slot is read from said second memory means (col.3 line 40 to col.4 line 25).

Regarding claim 5, Yamazaki discloses that selector means for switching data of a time slot directly input from an input line with data of a time slot read from said second memory means and outputting a switching result, wherein said selector means is controlled to output time slot information not to be switched as time slot data of an output frame without performing a process on the information by inputting information read from said first memory means as a selector signal to said selector means, and to

output time slot data read from said second memory means as time slot data of an output frame to be switched, figure 1.

Regarding claim 8, Yamazaki discloses a cross-connection switch comprising:

a counter counting a number of input time slots of an input frame in synchronization with the input frame, and outputting the count value as an input address and a write address, col.2 lines 15-55;

a first memory storing switching information data for a time slot, said data stored corresponding to addresses to which time slot information is assigned and outputting said switching information data according to the read address form said counter, col.2 lines 15-55;

second memory storing data of each time slot of an input frame in time slot units according to the write address from said counter and outputting said stored data of each time slot as read utilizing the switching information data from said first memory as a read address, thereby outputting time slot data of an output frame (col.2 lines 15-55, figure1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishihara et al (U.S Patent No 6,021,135) in the view of Yamazaki (U.S Patent No. 4,841,522).

Regarding claim 1, Ishihara discloses a cross-connection switch comprising:

management memory table 27 (first memory means) for storing data indicating switching information of a time slot at an address to which time slot information is assigned (col.9 line 56);

memory 25 (second memory means) for storing data of each time slot of an input frame in time slot units, inputting data stored in said first memory means, and outputting the data stored at the address specified by the data as time slot data of an output frame (col.9 lines 35-40, 54); and

counter means for counting a number of input time slots of an input frame, and outputting the count value as a read address and a write address respectively to said first memory means and said second memory means. See col.9 lines 50-65, col.10 lines 30-40).

Ishihara does not disclose an input frame in synchronization with an input frame. Yamazaki discloses counter 28 synchronizing with input signals and output signals, col.2 lines 15-40. Therefore, it would have been obvious to one having ordinary skill in the art to have the feature of the input frame in synchronization with the input frame to improve the problem of lagging the leading of signals between input and output switching so that the switch can process data signal properly.

Regarding claim 2, Ishihara discloses a multiplexed line signal having an input frame of n bits per channel is processed, a time slot number of each bit of an n-bit channel is assigned to addresses of said first memory means, and data indicating switching information about a time slot of each piece of bit data is entered at each address of said second memory means. See col.14 lines 30-40, col.9 lines 40-65.

Regarding claim 3, Ishihara discloses a plurality of lines are accommodated by said cross-connection switch, any line of the plurality of lines is selected for a switching process by entering switching information about time order of data of a time slot and switching information data between lines at each address of said first memory means. See col.7 lines 15-35.

Regarding claim 4, Ishihara discloses that information of a current input time slot is written to said second memory means, data to be used in processing one time slot before the current input time slot is read from said first memory means, a read address is output from said first memory means to said second memory means, and time slot data used in processing the one time slot before the current input time slot is read from said second memory means. See col.10 lines 25-45.

Regarding claim 5, Ishihara discloses that selector means for switching data of a time slot directly input from an input line with data of a time slot read from said second memory means and outputting a switching result, wherein said selector means is controlled to output time slot information not to be switched as time slot data of an output frame without performing a process on the information by inputting information read from said first memory means as a selector signal to said selector means, and to

output time slot data read from said second memory means as time slot data of an output frame to be switched. See col.8 lines 25-50.

Regarding claim 8, Ishihara discloses a cross-connection switch comprising:

a counter counting a number of input time slots of an input frame, and outputting the count value as an input address of buffer 25, figure 10 (read address) and switch to a different buffer 25 of different AAL processing part (write address), refer to figures 10, 12, and col.10 lines 20-65;

a first memory storing switching information data for a time slot, said data stored corresponding to addresses to which time slot information is assigned and outputting said switching information data according to the read address form said counter;

an address management table 27 (second memory) storing data of each time slot of an input frame in time slot units according to the write address from said counter and outputting said stored data of each time slot as read utilizing the switching information data from said first memory as a read address, thereby outputting time slot data of an output frame. See figures 10, 12, and col.10 lines 20-65.

Ishihara does not disclose an input frame in synchronization with an input frame. Yamazaki discloses counter 28 synchronizing with input signals and output signals, col.2 lines 15-40. Therefore, it would have been obvious to one having ordinary skill in the art to have the feature of the input frame in synchronization with the input frame to improve the problem of lagging the leading of signals between input and output switching so that the switch can process data signal properly.

Allowable Subject Matter

4. Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Thien Tran whose telephone number is (571) 272-3156. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

Thien Tran

STEVEN NGUYEN
PRIMARY EXAMINER